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(54) **DEVICE AND METHOD FOR PULSE CHARGING A BATTERY AND FOR DRIVING OTHER DEVICES WITH A PULSE**

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(57) **ABSTRACT**

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A two-phase solid-state battery charger can receive input energy from a variety of sources including AC current, a battery, a DC generator, a DC-to-DC inverter, solar cells or any other compatible source of input energy. Phase I is the charge phase and phase II the discharge phase wherein a signal or current passes through a dual timing switch that controls independently two channels dividing the two phases. The dual timing switch is controlled by a logic chip or pulse width modulator. A potential charge is allowed to build up in a capacitor bank, the capacitor bank is then disconnected from the energy input source and then pulse charged at high voltage into the battery to receive the charge. The momentary disconnection of the capacitor from the input energy source allows for a free-floating potential charge in the capacitor. Once the capacitor has completed discharging the potential charge into the battery, the capacitor disconnects from the battery and re-connects to the energy source thus completing the two-phase cycle.

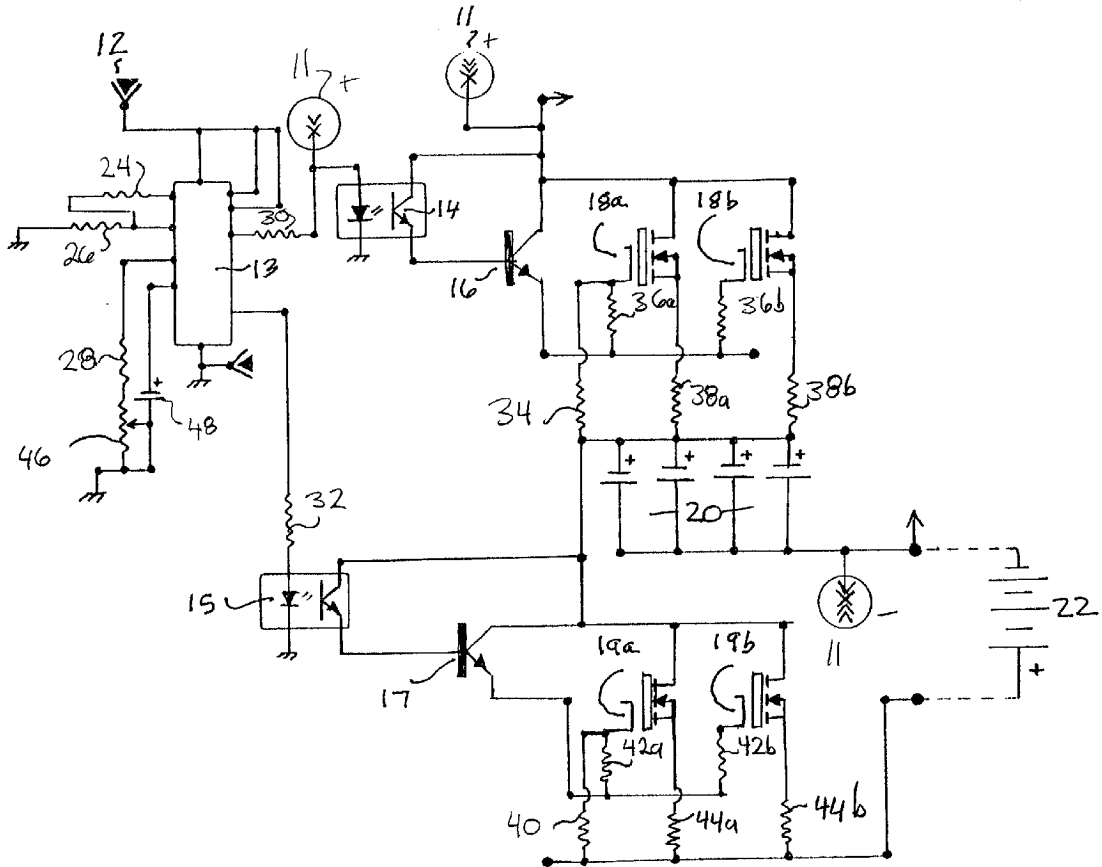
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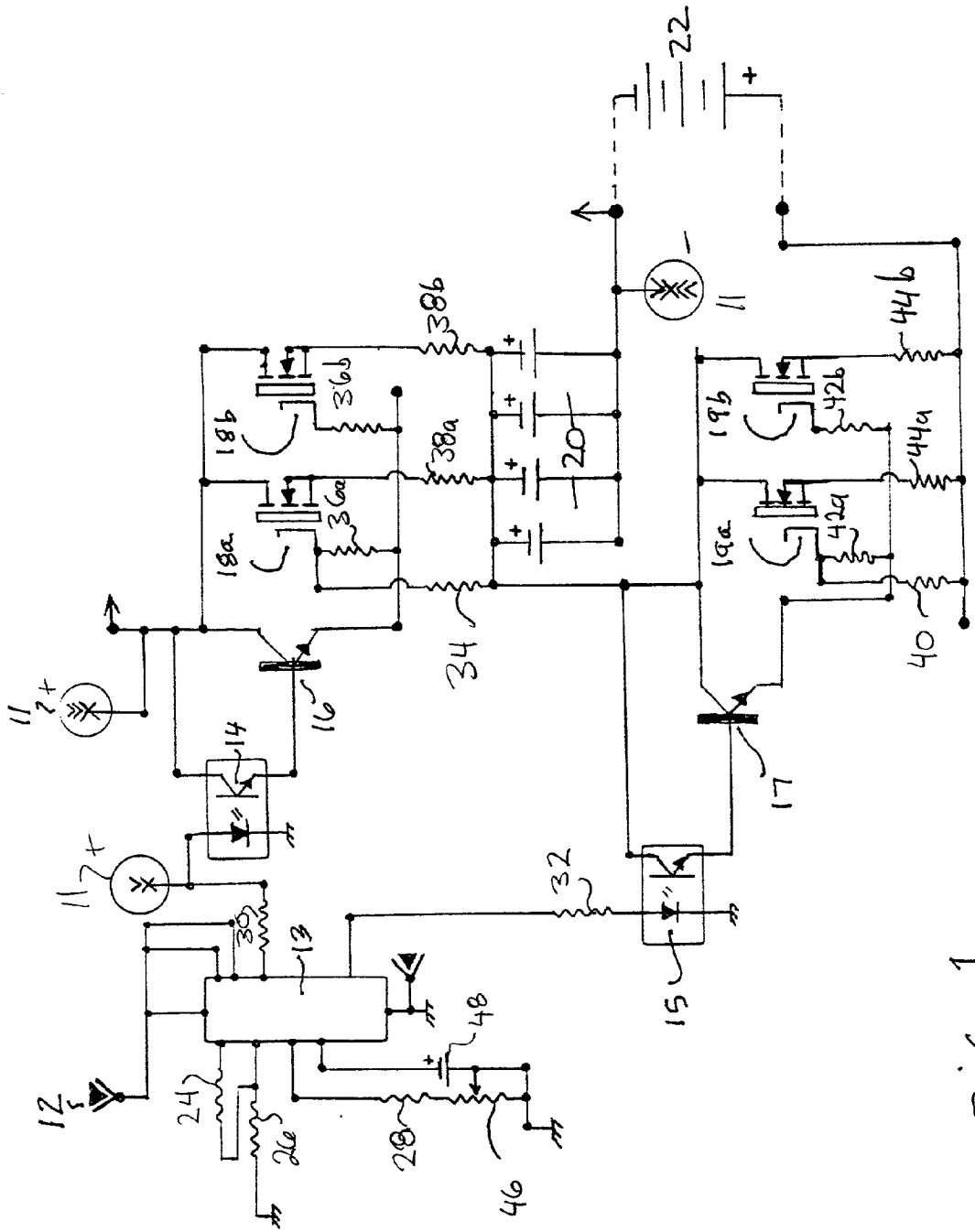


FIG. 1

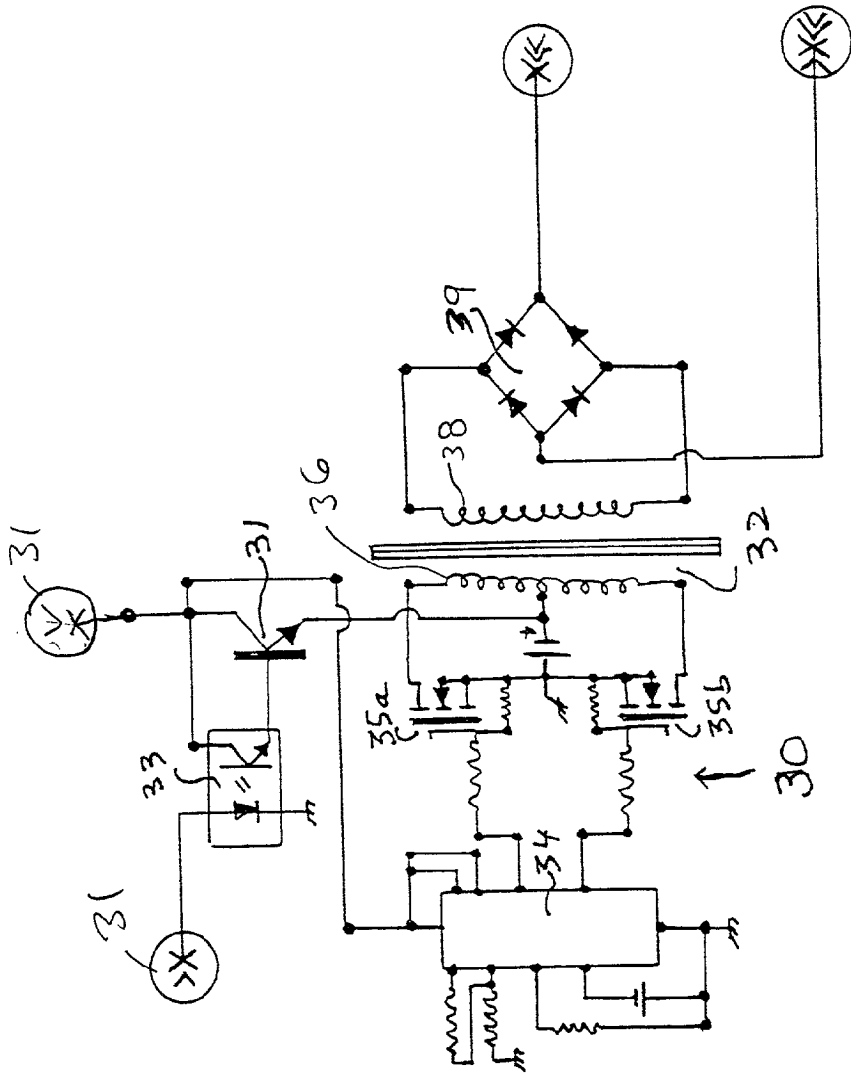


FIG. 2

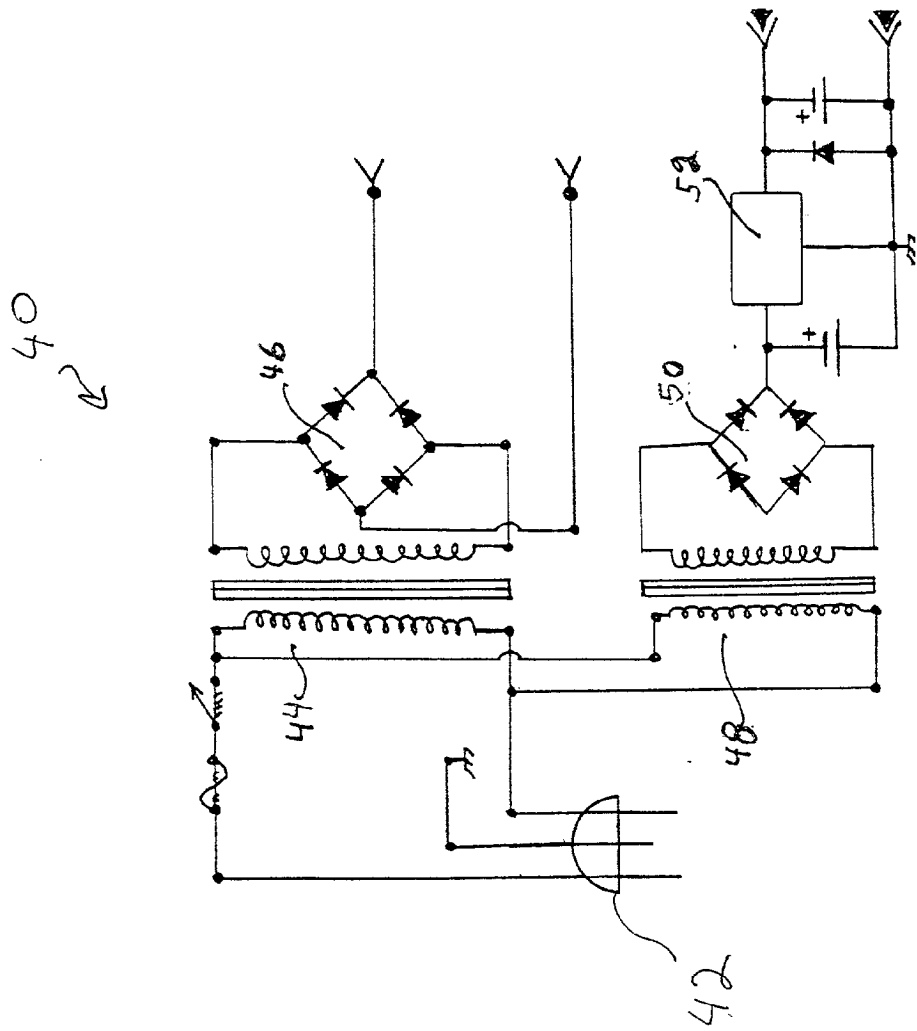


FIG. 3

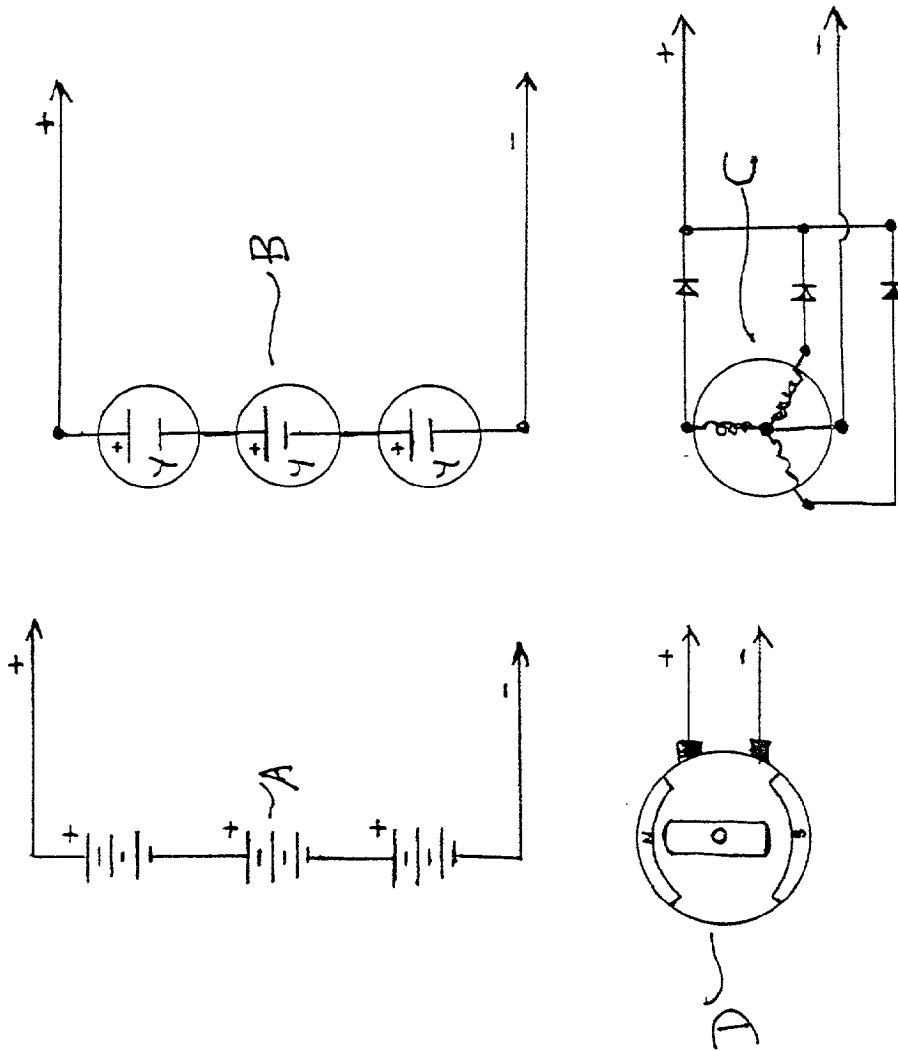


FIG. 4A-D

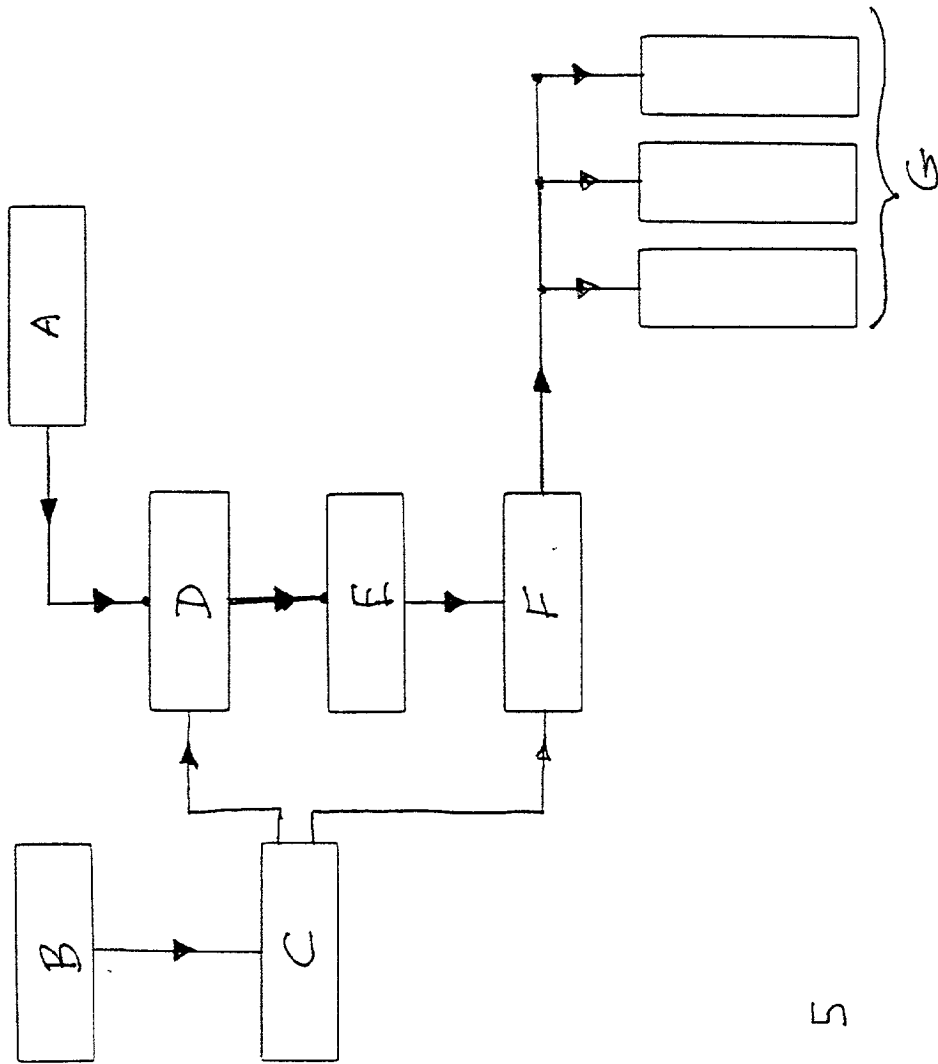


FIG. 5

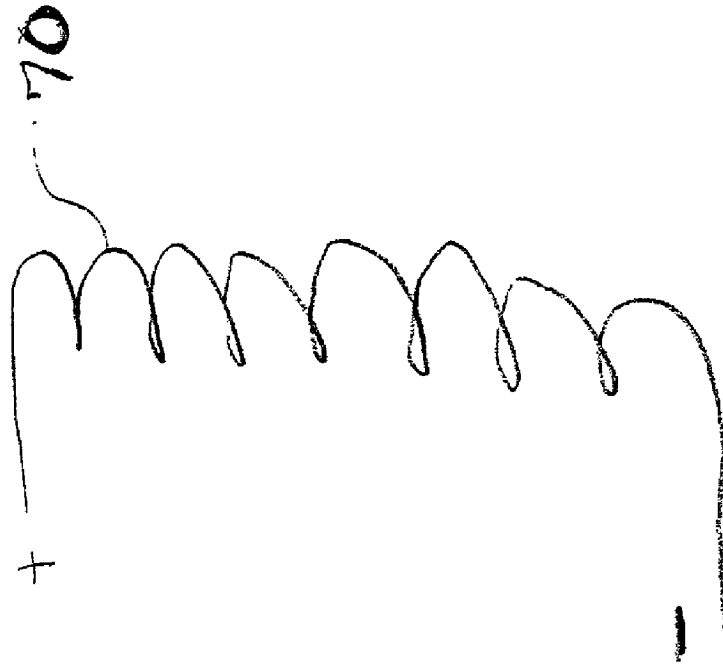


FIG. 7

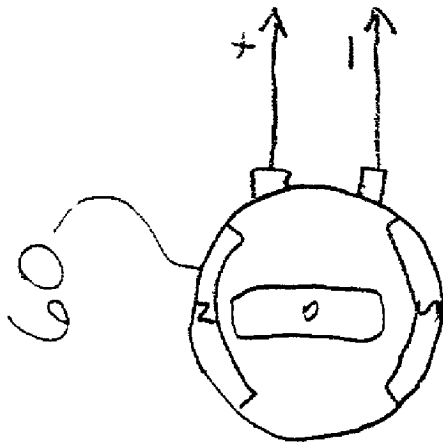


FIG. 6

DEVICE AND METHOD FOR PULSE CHARGING A BATTERY AND FOR DRIVING OTHER DEVICES WITH A PULSE

TECHNICAL FIELD

[0001] The invention relates generally to a battery pulse charger using a solid-state device and method wherein the current going to the battery is not constant. The signal or current is momentarily switch-interrupted as it flows through either the first channel, the charge phase, or the second channel, the discharge phase. This two-phase cycle alternates the signal in the two channels thereby allowing a potential charge in a capacitor to disconnect from its power source an instant before the capacitor discharges its stored potential energy into a battery for receiving the capacitor's stored energy. The capacitor then disconnects from the battery and re-connects to the power source upon completion of the discharge phase, thereby completing charge-discharge cycle. The battery pulse charger can also drive devices, such as a motor and a heating element, with pulses.

BACKGROUND AND PRIOR ART

[0002] Present day battery chargers use a constant charge current in their operation with no momentary disconnection of the signal or current as it flows either: 1) from a primary energy source to the charger; or 2) from the charger itself into a battery for receiving the charge. Some chargers are regulated to a constant current by any of several methods, while others are constant and are not regulated. There are no battery chargers currently in the art or available wherein there is a momentary signal or current disconnection between the primary energy source and the charger capacitors an instant before the capacitors discharge the stored potential energy into a battery receiving the pulse charge. Nor are there any chargers in the art that disconnect the charger from the battery receiving the charge when the charger capacitors receive energy from the primary source. The momentary current interruption allows the battery a short "rest period" and requires less energy from the primary energy source while putting more energy into the battery receiving the charge while requiring a shorter period of time.

SUMMARY OF THE INVENTION

[0003] One aspect of the invention relates to a solid-state device and method for creating a pulse current to pulse charge a battery or a bank of batteries in which a new and unique method is used to increase and preserve for a longer period of time the energy stored in the battery as compared to constant-current battery chargers. The device uses a timed pulse to create a waveform in a DC pulse to be discharged into the battery receiving the charge.

[0004] One embodiment of the Invention uses a means for dual switching such as a pulse width modulator (PWM), for example, a logic chip SG3524N PWM, and a means for optical coupling to a bank of high-energy capacitors to store a timed initial pulse charge. This is the charge phase, or phase I. The charged capacitor bank then discharges the stored high energy into the battery receiving the charge in timed pulses. Just prior to discharging the stored energy into the battery, the capacitor bank is momentarily disconnected from the power source, thus completing the charge phase, and thereby leaving the capacitor bank as a free-floating

potential charge disconnected from the primary energy source to then be discharged into the battery. The transfer of energy from the capacitor bank to the battery completes the discharge phase, or phase II. The two-phase cycle now repeats itself.

[0005] This embodiment of the battery pulse charger works by transferring energy from a source, such as an AC source, to an unfiltered DC source of high voltage to be stored in a capacitor or a capacitor bank. A switching regulator is set to a timed pulse, for example, a one second pulse that is 180 degrees out of phase for each set of switching functions. The first function is to build the charge in the capacitor bank from the primary energy source; the second function is to disconnect the power source from the capacitor bank; the third function is to discharge the stored high voltage to the battery with a high voltage spike in a timed pulse, for example, a one second pulse; and the fourth function is to re-connect the capacitor bank to the primary energy source. The device operates through a two-channel on/off switching mechanism or a gauging/re-gauging function wherein the charger is disconnected from its primary energy source an instant before the pulse charger discharges the high-energy pulse into the battery to be charged. As the primary charging switch closes, the secondary discharging switch opens, and visa-versa in timed pulses to complete the two phase cycle.

[0006] The means for a power supply is varied with several options available as the primary energy source. For example, primary input energy may come from an AC source connected into the proper voltage (transformer); from an AC generator; from a primary input battery; from solar cells; from a DC-to-DC inverter; or from any other adaptable source of energy. If a transformer means is the source of primary input energy, it can be a standard rectifying transformer used in power supply applications or any other transformer means applicable to the desired function. For example, it can be a 120-volt to 45-volt AC step-down transformer, and the rectifier can be a full-wave bridge of 200 volts at 20 amps, which is unfiltered when connected to the output of the transformer. The positive output terminal of the bridge rectifier is connected to the drains of the parallel field-effect transistors, and the negative terminal is connected to the capacitor bank negative.

[0007] The Field Effect Transistor (FET) switches can be IRF260 FETs, or any other FET means to accomplish this function. All are in parallel to achieve the proper current of the pulses. Each FET may be connected through a 7-watt, 0.05-ohm resistor with a common bus connection at the source. All the FET gates may be connected through a 240-ohm resistor to a common bus. There also may be a 2 K-ohm resistor between the gates and the drain bus.

[0008] A transistor means, for example an MJE15024 transistor, as a driver for the gates, drives the bus and in turn, an optical coupler drives the driver transistor through the first channel. A first charging switch is used to charge the capacitor bank, which acts as a DC potential source to the battery. The capacitor bank is then disconnected from the power rectifier circuit. The pulse battery charger is then transferred to a second field effect switch through the second channel for the discharge phase. The discharge phase is driven by a transistor, the transistor driven by an optical coupler. With a second or discharge switch on, the capacitor

bank potential charge is discharged into the battery to receive the charge. The battery receiving the charge is then disconnected from the pulse charger capacitor bank to repeat the cycle. The pulse charger may have any suitable source of input power including: 1) solar panels to raise the voltage to the capacitor bank; 2) a wind generator; 3) a DC-to-DC inverter; 4) an alternator; 5) an AC motor generator; 6) a static source such as a high voltage spark; and 7) other devices that can raise the potential of the capacitor bank.

[0009] In another embodiment of the invention, one can use the pulse charger to drive a device such as a motor or heating element with pulses of energy.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a schematic drawing of a solid-state pulse charger according to an embodiment of the invention.

[0011] FIG. 2 is a schematic drawing of a conventional DC-to-DC converter that can be used to provide power to the pulse charger of FIG. 1 according to an embodiment of the invention.

[0012] FIG. 3 is a schematic drawing of a conventional AC power supply that can be used to provide power to the pulse charger of FIG. 1 according to an embodiment of the invention.

[0013] FIGS. 4A-D are schematic drawings of other conventional power supplies that can be used to provide power to the pulse charger of FIG. 1 according to an embodiment of the invention.

[0014] FIG. 5 is a block diagram of the solid-state pulse charger of FIG. 1 according to an embodiment of the invention.

[0015] FIG. 6 is a diagram of a DC motor that the pulse charger of FIG. 1 can drive according to an embodiment of the invention.

[0016] FIG. 7 is a diagram of a heating element that the pulse charger of FIG. 1 can drive according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] An embodiment of the present invention is a device and method for a solidstate pulse charger that uses a stored potential charge in a capacitor bank. The solidstate pulse charger comprises a combination of elements and circuitry to capture and store available energy into a capacitor bank. The stored energy in the capacitors is then pulse charged into the battery to be charged. In one version of this embodiment, there is a first momentary disconnection between the charger and the battery receiving the charge during the charge phase of the cycle, and a second momentary disconnection between the charger and the input energy source during the discharge phase of the cycle.

[0018] As a starting point and an arbitrary method in describing this device and method, the flow of an electrical signal or current will be tracked from the primary input energy to final storage in the battery receiving the pulse charge.

[0019] FIG. 1 is a schematic drawing of the solid-state pulse charger according to an embodiment of the invention.

As shown in FIG. 1, the primary input energy source to the pulse charger is a power supply 11, examples of which are shown in FIGS. 2, 3, 4A-4D. A 12-volt battery, as a low voltage energy source 12, drives a dual switching means of control such as a logic chip or a pulse width modulator (PWM) 13. Alternatively, the voltage from the power supply 11 may be converted to a voltage suitable to power the PWM 13. The PWM 13 may be an SG3524N logic chip, and functions as an oscillator or timer to drive a 2-channel output with "on/off" switches that are connected when on to either a first optical isolator 14, or in the alternative, to a second optical isolator 15. The first and second optical isolators 14 and 15 may be H11D3 optical isolators. When the logic chip 13 is connected to a first channel, it is disconnected from a second channel, thus resulting in two phases of signal direction; phase I, a charge phase, and phase II, a discharge phase. When the logic chip 13 is switched to the charge phase, the signal flows to the first optical isolator 14. From the optical isolator 14, the signal continues its flow through a first NPN power transistor 16 that activates an N-channel MOSFET 18a and an N-channel MOSFET 18b. Current flowing through the MOSFETs 18a and 18b builds up a voltage across a capacitor bank 20, thereby completing the charge phase of the switching activity. The discharge phase begins when the logic chip 13 is switched to the second channel, with current flowing to the second optical isolator 15 and then through a second NPN power transistor 17, which activates an N-channel MOSFET 19a and an N-channel MOSFET 19b. After the logic chip 13 closes the first channel and opens the second channel, the potential charge in the capacitor bank 20 is free floating between the power supply 11, from which the capacitor bank 20 is now disconnected, and then connected to a battery 22 to receive the charge. It is at this point in time that the potential charge in the capacitor bank 20 is discharged through a high-energy pulse into the battery 22 or, a bank (not shown) of batteries. The discharge phase is completed once the battery 22 receives the charge. The logic chip 13 then switches the second channel closed and opens the first channel thus completing the charge-discharge cycle. The cycle is repetitive with the logic chip 13 controlling the signal direction into either channel one to the capacitor bank, or to channel two to the battery 22 from the capacitor bank. The battery 22 is given a momentary rest period without a continuous current during the charge phase.

[0020] The component values for the described embodiment are as follows. The resistors 24, 26, . . . 44b have the following respective values: 4.7K Ω , 4.7K Ω , 47K Ω , 330 Ω , 330 Ω , 2K Ω , 47 Ω , 47 Ω , 0.05 Ω (7 W), 0.05 Ω (7W), 2K Ω , 47 Ω , 47 Ω , 0.05 Ω (7 W), and 0.05 Ω (7W). The potentiometer 46 is 10K Ω , the capacitor 48 is 22 μ F, and the total capacitance of the capacitor bank 20 is 0.132F. The voltage of the battery 22 is between 12-24 V, and the voltage of the power supply 11 is 24-50 V such that the supply voltage is approximately 12-15 V higher than the battery voltage.

[0021] Other embodiments of the pulse charger are contemplated. For example, the bipolar transistors 16 and 17 may be replaced with field-effect transistors, and the transistors 18a, 18b, 19a, and 19b may be replaced with bipolar or insulated-gate bipolar (IGBT) transistors. Furthermore, one can change the component values to change the cycle time, the peak pulse voltage, the amount of charge that the capacitor bank 20 delivers to the battery 22, etc. In addition,

the pulse charger can have one or more than two transistors **18a** and **18b**, and one or more than two transistors **19a** and **19b**.

[0022] Still referring to **FIG. 1**, the operation of the above-discussed embodiment of the pulse charger is discussed.

[0023] To begin the first phase of the cycle during which the capacitor bank **20** is charged, the logic circuit **13** deactivates the isolator **15** and activates the isolator **14**. Typically, the circuit **13** is configured to deactivate the isolator **15** before or at the same time that it activates the isolator **14**, although the circuit **13** may be configured to deactivate the isolator **15** after it activates the isolator **14**.

[0024] Next, the activated isolator **14** generates a base current that activates the transistor **16**, which in turn generates a current that activates the transistors **18a** and **18b**.

[0025] The activated transistors **18a** and **18b** charge the capacitors in the bank **20** to a charge voltage equal or approximately equal to the voltage of the power supply **11** less the lowest threshold voltage of the transistors **18a** and **18b**. To begin the second phase of the cycle during which the capacitor bank **20** pulse charges the battery **22**, the logic circuit **13** deactivates the isolator **14** and activates the isolator **15**. Typically, the circuit **13** is configured to deactivate the isolator **14** before or at the same time that it activates the isolator **15**, although the circuit **13** may be configured to deactivate the isolator **14** after it activates the isolator **15**.

[0026] Next, the activated isolator **15** generates a base current that activates the transistor **17**, which in turn generates a current that activates the transistors **19a** and **19b**.

[0027] The activated transistors **19a** and **19b** discharge the capacitors in the bank **20** into the battery **22** until the voltage across the bank **20** is or is approximately equal to the voltage across the battery **22** plus the lowest threshold voltage of the transistors **19a** and **19b**. Alternatively, the circuit **13** can deactivate the isolator **15** at a time before the bank **20** reaches this level of discharge. Because the resistances of the transistors **19a** and **19b**, the resistors **44a** and **44b**, and the battery **22** are relatively low, the capacitors in the bank **20** discharge rather rapidly, thus delivering a pulse of current to charge the battery **22**. For example, where the pulse charger includes components having the values listed above, the bank **20** delivers a pulse of current having a duration of or approximately of 100 ms and a peak of or approximately of 250 A.

[0028] **FIG. 2** is a schematic drawing of a conventional DC-to-DC converter **30** that can be used as the power supply **11** of **FIG. 1** according to an embodiment of the invention. A DC-to-DC converter converts a low DC voltage to a higher DC voltage or vice-versa. Therefore, such a converter can convert a low voltage into a higher voltage that the pulse charger of **FIG. 1** can use to charge the capacitor bank **20** (**FIG. 1**). More specifically, the converter **30** receives energy from a source **31** such as a 12-volt battery. An optical isolator sensor **33** controls an NPN power transistor **31**, which provides a current to a primary coil **36** of a power transformer **32**. A logic chip or pulse width modulator (PWM) **34** alternately switches on and off an IRF260 first N-channel MOSFET **35a** and an IRF260 second N-channel MOSFET **35b** such that when the MOSFET **35a** is on the

MOSFET **35b** is off and vice-versa. Consequently, the switching MOSFETs **35a** and **35b** drive respective sections of the primary coil **36** to generate an output voltage across a secondary coil **38**. A full-wave bridge rectifier **39** rectifies the voltage across the secondary coil **38**, and this rectified voltage is provided to the pulse charger of **FIG. 1**. Furthermore, the secondary coil **38** can be tapped to provide a lower voltage for the PWM **13** of **FIG. 1** such that the DC-to-DC converter **30** can be used as both the power supply **11** and the low-voltage supply **12** of **FIG. 1**.

[0029] **FIG. 3** is a schematic drawing of an AC power supply **40** that can be used as both the power supply **11** and the power supply **12** of **FIG. 1** according to an embodiment of the invention. The power input **42** to the supply **40** is 120 VAC. A first transformer **44** and full-wave rectifier **46** compose the supply **11**, and a second transformer **48**, full-wave rectifier **50**, and voltage regulator **52** compose the supply **12**.

[0030] **FIGS. 4A-D** are schematic drawings of various conventional primary energy input sources that can be used as the supply **11** and/or the supply **12** of **FIG. 1** according to an embodiment of the invention. **FIG. 4A** is a schematic drawing of serially coupled batteries; **FIG. 4B** is a schematic drawing of serially coupled solar cells; **FIG. 4C** is a schematic drawing of an AC generator; and **FIG. 4D** is a schematic drawing of a DC generator.

[0031] **FIG. 5** is a block diagram of the solid-state pulse charger of **FIG. 1** according to an embodiment of the invention. Block A is the power supply **11**, which can be any suitable power supply such as those shown in **FIGS. 2, 3, 4A-4D**. Block B is the power supply **12**, which can be any suitable power supply such as a 12 VDC supply or the supply shown in **FIG. 3**. Block C is the PWM **13** and its peripheral components. Block D is the charge switch that includes the first optical isolator chip **14**, the first NPN power transistor **16**, the first set of two N-channel MOSFETs **18a** and **18b**, and their peripheral resistors. Block E is the capacitor bank **20**. Block F is the discharge switch that includes the second optical isolator chip **15**, the second NPN power transistor **17**, the second set of two N-channel MOSFETs **19a** and **19b**, and their peripheral resistors. Block G is the battery **22** that is being pulse charged.

[0032] A unique feature that distinguishes one embodiment of the above-described pulse charger from conventional chargers is the method charging the battery with pulses of current instead of with a continuous current. Consequently, the battery is given a reset period between pulses.

[0033] **FIG. 6** is a diagram of a DC motor **60** that the pulse charger of **FIG. 1** can drive according to an embodiment of the invention. Specifically, one can connect the motor **60** in place of the battery **22** (**FIG. 1**) such that the pulse charger drives the motor with pulses of current. Although one need not modify the pulse charger to drive the motor **60**, one can modify the pulse charger to make it more efficient for driving the motor. For example, one can modify the values of the resistors peripheral to the PWM **13** (**FIG. 1**) to vary the width and peak of the drive pulses from the capacitor bank **20** (**FIG. 1**).

[0034] **FIG. 7** is a diagram of a heating element **70**, such as a dryer- or water-heating element, that the pulse charger

of FIG. 1 can drive according to an embodiment of the invention. Specifically, one can connect the heating element 70 in place of the battery 22 (FIG. 1) such that the pulse charger drives the element with pulses of current. Although one need not modify the pulse charger to drive the element 70, one can modify the pulse charger to make it more efficient for driving the element. For example, one can modify the values of the resistors peripheral to the PWM 13 (FIG. 1) to vary the width and peak of the drive pulses from the capacitor bank 20 (FIG. 1).

[0035] In the embodiments discussed above, specific electronic elements and components are used. However, it is known that a variety of available transistors, resistors, capacitors, transformers, timing components, optical isolators, pulse width modulators, MOSFETs, and other electronic components may be used in a variety of combinations to achieve an equivalent result. Finally, although the invention has been described with reference of particular means, materials and embodiments, it is to be understood that the invention is not limited to the particulars disclosed and extends to all equivalents within the scope of the claims.

What is claimed is:

1. A solid-state pulse battery charger wherein input power from a primary source is stored as a potential charge in a capacitor bank, said capacitor bank then disconnected from said input power source through a dual timing means, said capacitor then connected to a battery to receive the potential charge, the charge then discharged into said battery from said capacitor, said battery then disconnected from said capacitor through said dual timing means, said capacitor then re-connected to said input power source completing a two phase switching cycle comprising:

- a. a means for providing input power;
 - b. a means for timing a signal and a current flow in two phases, a charge phase and a discharge phase, through either a first channel output for charging said capacitor bank, or a second channel output for discharging stored energy from said capacitor into said battery, the current flowing from said first channel output through a first optical isolator and through a first NPN power transistor, said first transistor activating a first pair of N-channel MOSFETs with voltage stored as the potential charge in said capacitor bank, said capacitor disconnecting from said input power means by said timing means;
 - c. said means for timing current flow connecting to said second channel output, current flowing from said second channel through a second optical isolator and through a second NPN power transistor, said second transistor activating a second pair of N-channel MOSFETs, said capacitor connecting to said battery, the potential charge discharging into said battery, said timing means disconnecting said capacitor from said battery, and connecting said capacitor to said power means.
2. The pulse charger of claim 1 wherein the means for providing input power is an AC voltage current.
 3. The pulse charger of claim 1 wherein the means for providing input power is a battery.
 4. The pulse charger of claim 1 wherein the means for providing input power is a DC generator.

5. The pulse charger of claim 1 wherein the means for providing input power is an AC generator.

6. The pulse charger of claim 1 wherein the means for providing input power is a solar cell.

7. The pulse charger of claim 1 wherein the means for providing input power is a DC-to-DC inverter.

8. The pulse charger of claim 1 wherein the means for timing a signal is a pulse width modulator, said modulator an SG3524N logic chip.

9. The pulse charger of claim 1 wherein the optical isolator is an H11D3 isolator.

10. The pulse charger of claim 1 wherein the NPN power transistor is an MJE15024 transistor.

11. The pulse charger of claim 1 wherein the N-channel MOSFET is a IRF260 MOSFET.

12. A solid-state pulsed battery charger wherein input power from a primary source is stored as a potential charge in a capacitor bank, said capacitor then disconnected from said input power source through a dual timing means, said capacitor then connected to a battery to receive the potential charge, the charge then discharged into said battery from said capacitor, said battery then disconnected from said capacitor through said dual timing means, said capacitor then reconnected to said input power source completing a two phase cycle comprising:

- a. a means for providing said input power, said means either an AC voltage current, or a battery, or a DC generator, or an AC generator, or a solar cell, or a DC-to-DC inverter;
 - b. a means for timing a signal and a current flow, said timing means a pulse width modulator, logic chip SG3524N, the current flowing through either a first channel output, or a second channel output, the current flowing from said first channel output through a first optical isolator, said isolator an H11D3, and through a first NPN power transistor, said transistor an MJE15024, said first transistor activating a first pair of N-channel MOSFETs, said MOSFETs an IRF260, with current voltage stored as the potential charge in said capacitor bank, said capacitor disconnecting from said input power means by said logic chip;
 - c. said timing logic chip connecting to said second channel output, current flowing from said second channel through a second optical isolator, said isolator an H11D3, and through a second NPN power transistor, said second transistor an MJE15024, and activating a second pair of N-channel MOSFETs, said MOSFETs an IRF260, with current voltage stored as the potential charge in said capacitor bank, said capacitor disconnecting from said input power means by said logic chip, said capacitor connecting to said battery, the potential charge discharging into said battery, said timing means disconnecting said capacitor from said battery and connecting said capacitor to said power means.
13. A method of making a solid-state pulse battery charger wherein input power from a primary source is stored as a potential charge in a capacitor bank, said capacitor disconnected from said input power source through a dual timing means, said capacitor connected to a battery to receive the potential charge, said charge discharged into said battery from said capacitor, said battery disconnected from said capacitor through said dual timing means, said capacitor

reconnected to said input power source completing a two phase cycle comprising the steps of:

- a. providing a source of input power;
 - b. connecting a means for dual-timing said charger to control a signal or current flow through a first channel output comprising a first optical isolator, a first NPN power transistor and a first pair of N-channel MOSFETs;
 - c. capturing energy from said current and storing said energy in said capacitor bank thereby charging said capacitor;
 - d. switching the flow of said current using said timing device to a second channel comprising a second optical isolator, a second NPN power transistor and a second pair of N-channel MOSFETs, thus disconnecting said capacitor from said power source and connecting said capacitor to said battery;
 - e. discharging the potential charge into said battery;
 - f. switching the flow of the current using said timing device to said power source and said first channel to complete said cycle.
14. The pulse charger of claim 13 wherein the means for providing input power is an AC voltage current.
15. The pulse charger of claim 13 wherein the means for providing input power is a battery.
16. The pulse charger of claim 13 wherein the means for providing input power is a DC generator.
17. The pulse charger of claim 13 wherein the means for providing input power is an AC generator.
18. The pulse charger of claim 13 wherein the means for providing input power is a solar cell.
19. The pulse charger of claim 13 wherein the means for providing input power is a DC-to-DC inverter.
20. The pulse charger of claim 13 wherein the means for timing a signal is a pulse width modulator, said modulator an SG3524N logic chip.
21. The pulse charger of claim 13 wherein the optical isolator is an H11D3 isolator.
22. The pulse charger of claim 13 wherein the NPN power transistor is an MJE15024 transistor.
23. The pulse charger of claim 13 wherein the N-channel MOSFET is a IRF260 MOSFET.
24. A battery charger, comprising:
- a supply node;
 - a charge node;
 - a switch circuit coupled to the supply and the charge nodes and operable to, allow a battery-charge current to flow into the charge node during a battery-charge period, and prohibit the battery-charge current from flowing into the charge node during a battery-rest period.
25. The battery charger of claim 24, further comprising:
- a charge-storage device coupled to the switch circuit; and wherein the switch circuit is operable to, allow the battery-charge current to flow from the charge-storage device into the charge node during the battery-charge period, and charge the charge-storage device during the battery-rest period.

26. The battery charger of claim 24, further comprising: a capacitor coupled to the switch circuit; and wherein the switch circuit is operable to, allow the battery-charge current to flow from the capacitor into the charge node during the battery-charge period, and charge the capacitor during the battery-rest period.
27. A method, comprising:
- charging a battery during a first period of a charge cycle; and
 - prohibiting the charging of the battery during a second period of the charge cycle.
28. The method of claim 27 wherein:
- charging the battery comprises charging the battery with a charge current during the first period of the charge cycle; and
 - prohibiting the charging of the battery comprises prohibiting the charge current from flowing into the battery during the second period of the charge cycle.
29. The method of claim 27 wherein:
- charging the battery comprises discharging a capacitor into the battery during the first period of the charge cycle; and
 - prohibiting the charging of the battery comprises uncoupling the capacitor from the battery during the second period of the charge cycle.
30. The method of claim 27, further comprising:
- wherein charging the battery comprises discharging a capacitor into the battery during the first period of the charge cycle;
 - wherein prohibiting the charging of the battery comprises uncoupling the capacitor from the battery during the second period of the charge cycle; and
 - charging the capacitor during the second period of the charge cycle.
31. A method, comprising:
- discharging a charge-storage device into a battery during a first period of a battery-charge cycle; and
 - uncoupling the charge-storage device from the battery and charging the charge-storage device during a second period of the battery-charge cycle.
32. The method of claim 31 wherein uncoupling the charge-storage device comprises uncoupling the charge-storage device from the battery before commencing charging of the charge-storage device.
33. The method of claim 31 wherein uncoupling the charge-storage device comprises uncoupling the charge-storage device from the battery after commencing charging of the charge-storage device.
34. The method of claim 31 wherein uncoupling the charge-storage device comprises simultaneously uncoupling the charge-storage device from the battery and commencing charging of the charge-storage device.